

## CLAIMS

What is claimed is:

1. A method for reducing transmitter emissions, the method comprising:
  - partitioning an encoder block into at least a first group of encoder processing cells and a second group of encoder processing cells;
  - partitioning a DAC block into at least a first group of DAC processing cells and a second group of DAC processing cells;
  - coupling said at least said first group of encoder processing cells with said at least said first group of DAC processing cells and said at least said second group of encoder processing cells with said at least said second group of DAC processing cells;
  - and
  - clocking said first group of encoder processing cells using a first clock signal and said second group of encoder processing cells using a second clock signal.
2. The method according to claim 1, further comprising grouping at least a portion of odd cells of said encoder block into said first group of encoder processing cells.
3. The method according to claim 2, further comprising grouping at least a portion of even cells of said encoder block into said second group of encoder processing cells.

4. The method according to claim 3, further comprising grouping at least a remaining portion of said odd cells of said DAC block into said first group of DAC processing cells.

5. The method according to claim 4, further comprising grouping at least a remaining portion of said even cells of said DAC block into said second group of DAC processing cells.

6. The method according to claim 5, further comprising processing an output of each of said odd cells of said first group of encoder processing cells by a corresponding one of said odd cells of said first group of DAC processing cells.

7. The method according to claim 6, further comprising processing an output of each of said even cells of said second group of encoder processing cells by a corresponding one of said even cells of said second group of DAC processing cells.

8. The method according to claim 7, further comprising aggregating an output of each of said even DAC processing cells and said odd DAC processing cells to create a reduced emissions output signal.

9. The method according to claim 8, further comprising low pass filtering said aggregated output.

10. The method according to claim 1, further comprising generating said second clock signal as a delayed version of said first clock signal.

11. A machine-readable storage having stored thereon, a computer program having at least one code section for reducing transmitter emissions, the at least one code section being executable by a machine for causing the machine to perform steps comprising:

partitioning an encoder block into at least a first group of encoder processing cells and a second group of encoder processing cells;

partitioning a DAC block into at least a first group of DAC processing cells and a second group of DAC processing cells;

coupling said at least said first group of encoder processing cells with said at least said first group of DAC processing cells and said at least said second group of encoder processing cells with said at least said second group of DAC processing cells;  
and

clocking said first group of encoder processing cells using a first clock signal and said second group of encoder processing cells using a second clock signal.

12. The machine-readable storage according to claim 11, further comprising at least code section for grouping at least a portion of odd cells of said encoder block into said first group of encoder processing cells.

13. The machine-readable storage according to claim 12, wherein said at least one grouping code section groups at least a portion of even cells of said encoder block into said second group of encoder processing cells.

14. The machine-readable storage according to claim 13, wherein said at least one grouping code section groups at least a remaining portion of said odd cells of said DAC block into said first group of DAC processing cells.

15. The machine-readable storage according to claim 14, wherein said at least one grouping code section groups at least a remaining portion of said even cells of said DAC block into said second group of DAC processing cells.

16. The machine-readable storage according to claim 15, further comprising at least one code section for processing an output of each of said odd cells of said first group of encoder processing cells by a corresponding one of said odd cells of said first group of DAC processing cells.

17. The machine-readable storage according to claim 16, wherein said at least one processing code section processes an output of each of said even cells of said second group of encoder processing cells by a corresponding one of said even cells of said second group of DAC processing cells.

18. The machine-readable storage according to claim 17, further comprising code for aggregating an output of each of said even DAC processing cells and said odd DAC processing cells to create a reduced emissions output signal.

19. The machine-readable storage according to claim 18, further comprising code for low pass filtering said aggregated output.

20. The machine-readable storage according to claim 11, further comprising code for generating said second clock signal as a delayed version of said first clock signal.

21. A system for reducing emissions transmitter, the system comprising:  
an encoder block partitioned into at least a first group of encoder processing cells and a second group of encoder processing cells;  
a DAC block partitioned into at least a first group of DAC processing cells and a second group of DAC processing cells;  
said at least said first group of encoder processing cells being coupled with said at least said first group of DAC processing cells and said at least said second group of encoder processing cells being coupled with said at least said second group of DAC processing cells; and

at least one clock generator adapted to generate a first clock signal for clocking said first group of encoder processing cells and a second clock signal for clocking said second group of encoder processing cells.

22. The system according to claim 21, wherein said first group of encoder processing cells comprises at least a portion of odd cells of said encoder block.

23. The system according to claim 22, wherein said second group of encoder processing cells comprises at least a portion of even cells of said encoder block.

24. The system according to claim 23, wherein said first group of DAC processing cells comprises at least a remaining portion of said odd cells of said DAC block.

25. The system according to claim 24, wherein said second group of DAC processing cells further comprises at least a remaining portion of said even cells of said DAC block.

26. The system according to claim 25, wherein,

an output of each of said odd cells of said first group of encoder processing cells is coupled to an input of a corresponding one of said odd cells of said first group of DAC processing cells; and

an output of each of said even cells of said second group of encoder processing cells is coupled to an input of a corresponding one of said even cells of said second group of DAC processing cells.

27. The system according to claim 26, further comprising an aggregator adapted to aggregate an output of each of said even DAC processing cells and said odd DAC processing cells to create a reduced emissions output signal.

28. The system according to claim 27, further comprising a low pass filter adapted to low pass filter said aggregated output.

29. The system according to claim 21, wherein said at least one clock generator is adapted to generate said second clock signal as a delayed version of said first clock signal.

30. The system according to claim 21, further comprising at least one waveform generator coupled to said encoder block.

31. The system according to claim 30, wherein said at least one waveform generator is a digital filter.

32. The system according to claim 30, wherein said at least one waveform generator, said encoder block and said DAC block is integrated within a chip.

33. The system according to claim 21, wherein said encoder block is a DAC encoder block.